ABSTRACT OF THE DISCLOSURE

A data processor arranged so that a block transfer control unit (12) can initiate block transfer in response to the execution of a particular instruction by a CPU, in order to increase the speed and efficiency of the data transfer between a CPU-accessible internal memory (5) and an external memory (25,26). When an address specified by the addressing field coincides with an address mapped to the internal memory, the particular instruction sets a logical address as one of the transfer source or transfer destination addresses of the data block transfer. The internal memory is allotted to a part of virtual address space; the internal memory allotted so is associated with the physical address space, to which the external memory set as the other address is allotted, by a process in which a TLB is used when the MMU is in ON, and a given register is used when the MMU is in OFF.